In re Patent Application of:
DEQUINA ET AL
Serial No. **10/725,764**
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In the Claims:

Claims 12.-19. (Canceled)

20. (New) A control circuit for a switch mode DC-DC converter comprising an arrangement of LGATE, UGATE and PHASE node condition threshold detectors, said LGATE condition threshold detector being operative to monitor the gate (LGATE) of a lower FET (LFET), said UGATE condition threshold detector being operative to monitor the gate (UGATE) of an upper FET (UFET), and said PHASE node condition threshold detector being operative to monitor a phase node voltage at a PHASE node or common node between said UFET and said LFET, voltage outputs of said threshold detectors being processed in accordance with a switching control operator to ensure that each of said UFET and said LFET is completely turned off before the other FET begins conduction, thereby maintaining a dead time that exhibits no shoot-through current and is independent of type of switching FET, and wherein said switching control operator is operative to trigger turn-on of said UFET, which causes the phase node voltage to increase from a first voltage level to a second voltage level higher than said first voltage level, in response to turn-off of said LFET, and in response to said phase node voltage at said PHASE node having reached a prescribed negative polarity voltage threshold following a predetermined blanking delay subsequent to said turn-off of said LFET.

21. (New) The control circuit according to claim 20, wherein said switching control operator is operative, in response to said PHASE node not having reached said prescribed negative polarity voltage following said predetermined blanking delay subsequent to turn-off of said LFET, to monitor whether said phase node voltage has increased from said first voltage level to a prescribed positive polarity voltage threshold and, in response to said phase node voltage having increased from said first voltage level to said prescribed positive polarity voltage threshold, said switching control operator is operative to trigger turn-on of said UFET, and thereby causing said phase node voltage to increase to said second voltage level.

22. (New) The control circuit according to claim 21, wherein said switching control operator is operative, in response to an elapse of a prescribed time-out without either of said prescribed positive and negative polarity voltage thresholds having been reached at said phase node following said blanking delay, to trigger turn-on of said UFET, causing said phase node voltage to increase from said first voltage level to said second voltage level.

23. (New) The control circuit according to claim 20, wherein said switching control operator is operative, in response to turn-off of said UFET, and in response to a UGATE voltage at said UGATE dropping to a voltage level that is a prescribed value above said

phase node voltage, to trigger a prescribed time out and then turn on said LFET in response to expiration of said prescribed time out.

24. (New) The control circuit according to claim 20, wherein said switching control operator is operative, in response to turn-off of said UFET, and in response to said phase node voltage reaching a predetermined threshold voltage, to turn on said LFET.

25. (New) A method for controlling a switch mode DC-DC converter comprising an upper FET (UFET), having an upper gate (UGATE), and a lower FET (LFET) having a lower gate (LGATE), said UFET and said LFET being coupled between power supply voltage rails, and having a common node or PHASE node therebetween, said method comprising the steps of:

(a) monitoring an LGATE voltage, a UGATE voltage and a phase node voltage; and

(b) in response to turn-off of said LFET, and in response to said phase node voltage at said PHASE node having reached a prescribed negative polarity voltage threshold following a predetermined blanking delay subsequent to said turn-off of said LFET, triggering turn-on of said UFET, thereby causing said phase node voltage to increase from a first voltage level to a second voltage level higher than said first voltage level.

26. (New) The method according to claim 25, wherein step (b)

further comprises, in response to said PHASE node not having reached said prescribed negative polarity voltage following said predetermined blanking delay subsequent to turn-off of said LFET, monitoring whether said phase node voltage has increased from said first voltage level to a prescribed positive polarity voltage threshold and, in response to said phase node voltage having increased from said first voltage level to said prescribed positive polarity voltage threshold, triggering turn-on of said UFET, thereby causing said phase node voltage to increase to said second voltage level.

27. (New) The method circuit according to claim 26, wherein step (b) further comprises, in response to an elapse of a prescribed time-out without either of said prescribed positive and negative polarity voltage thresholds having been reached at said phase node following said blanking delay, triggering turn-on of said UFET, thereby causing said phase node voltage to increase from said first voltage level to said second voltage level.